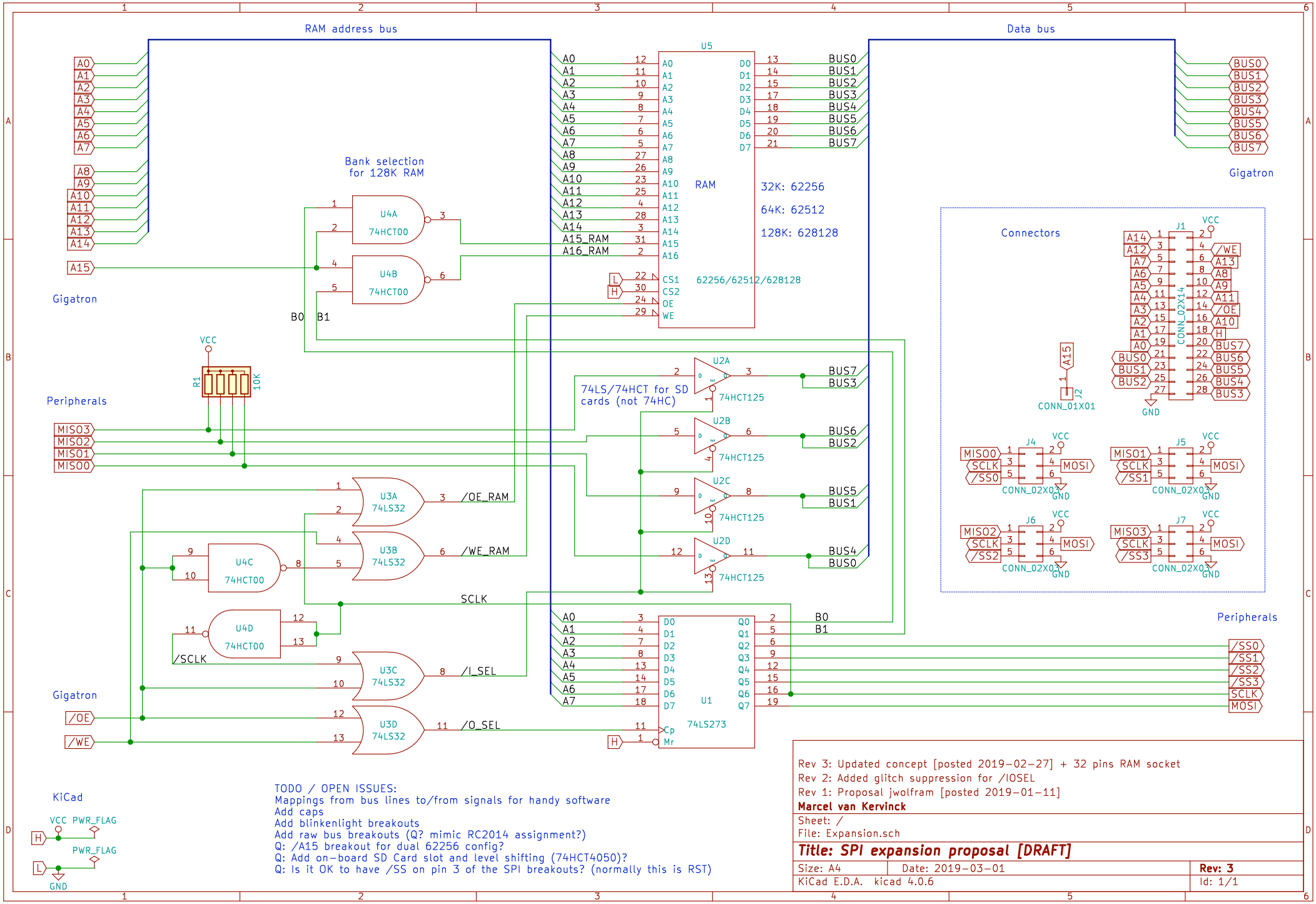
RAM address bus
Data bus
Bank selection
for 128K RAM
Gigatron
Peripherals
Connectors
74LS/74HCT for SD
cards (not 74HC)
RAM
32K: 62256
64K: 62512
128K: 628128
62256/62512/628128
U5
U1
74LS273
U4A
U4B
U4C
U4D
U3A
U3B
U3C
U3D
U2A
U2B
U2C
U2D
74HCT00
74LS32
74HCT125
R1
10K
VCC
GND
J1
J2
J4
J5
J6
J7
CONN_02X14
CONN_01X01
CONN_02X03
/OE_RAM
/WE_RAM
/I_SEL
/O_SEL
SCLK
/SCLK
MISO3
MISO2
MISO1
MISO0
MOSI
/SS0
/SS1
/SS2
/SS3
BUS0
BUS1
BUS2
BUS3
BUS4
BUS5
BUS6
BUS7
B0
B1
/OE
/WE
KiCad
VCC PWR_FLAG
PWR_FLAG
GND
TODO / OPEN ISSUES:
Mappings from bus lines to/from signals for handy software
Add caps
Add blinkenlight breakouts
Add raw bus breakouts (Q? mimic RC2014 assignment?)
Q: /A15 breakout for dual 62256 config?
Q: Add on-board SD Card slot and level shifting (74HCT4050)?
Q: Is it OK to have /SS on pin 3 of the SPI breakouts? (normally this is RST)
Rev 3: Updated concept [posted 2019-02-27] + 32 pins RAM socket
Rev 2: Added glitch suppression for /IOSEL
Rev 1: Proposal jwolfram [posted 2019-01-11]
Marcel van Kervinck
Sheet: /
File: Expansion.sch
Title: SPI expansion proposal [DRAFT]
Size: A4
Date: 2019-03-01
Rev: 3
KiCad E.D.A. kicad 4.0.6
Id: 1/1